L Number	Hits	Search Text	DB	Time stamp
1	1	("6613695").PN.	USPAT; US-PGPUB	2004/05/27 16:13
2	1	("5950107").PN.	USPAT; US-PGPUB	2004/05/27 16:13
3	1	("6200866").PN.	USPAT; US-PGPUB	2004/05/27 16:19
4	182	(gate or electrode) and ((gate near3 dielectric) same plasma same nitrogen)	USPAT; US-PGPUB	2004/05/27 16:24
5	12	((gate or electrode) and ((gate near3 dielectric) same plasma same nitrogen)) and ALD	USPAT; US-PGPUB	2004/05/27 16:25
6	1	(((gate or electrode) and ((gate near3 dielectric) same plasma same nitrogen)) and ALD) and @ad<20001124	USPAT; US-PGPUB	2004/05/27 16:26
7	214	(gate or electrode) and ((gate near3 dielectric) same plasma same ("N.sub.2" or "NH.sub.3" or NO or "N.sub.2O"))	USPAT; US-PGPUB	2004/05/27 16:25
8	10	((gate or electrode) and ((gate near3 dielectric) same plasma same ("N.sub.2" or "NH.sub.3" or NO or "N.sub.2O"))) and ALD	USPAT; US-PGPUB	2004/05/27 16:26
9	1	(((gate or electrode) and ((gate near3 dielectric) same plasma same ("N.sub.2" or "NH.sub.3" or NO or "N.sub.2O"))) and ALD) and @ad<20001124	USPAT; US-PGPUB	2004/05/27 16:26
10	114	((gate or electrode) and ((gate near3 dielectric) same plasma same ("N.sub.2" or "NH.sub.3" or NO or "N.sub.2O"))) and @ad<20001124	USPAT; US-PGPUB	2004/05/27 16:35

US-PAT-NO: 5837598

DOCUMENT-IDENTIFIER: US 5837598 A

TITLE: Diffusion barrier for polysilicon gate electrode of MOS device in integrated circuit structure, and method of making same

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Brief Summary Text - BSTX (16):

In accordance with the invention, a thin polysilicon gate electrode is doped in a manner in which the underlying gate oxide and semiconductor substrate is not penetrated by the dopant, by forming a dopant barrier at the polysilicon/gate dielectric interface. The polysilicon gate electrode of an MOS device, forming a part of an integrated circuit structure on a semiconductor substrate, is uniformly doped by first forming a very thin layer of amorphous or polycrystalline silicon, e.g., from about 2 nm to about 10 nm, over a gate oxide layer. The structure is then exposed to a nitrogen **plasma** formed from N.sub.2 at a power level sufficient to break the silicon--silicon bonds in the thin layer of silicon, but insufficient to cause sputtering of the silicon, resulting in the formation of a barrier layer containing silicon and nitrogen at the surface of the thin silicon layer. Polysilicon is then deposited over the barrier layer to the desired thickness of the polysilicon gate electrode. The polysilicon gate electrode is then conventionally doped, i.e., by implantation followed by furnace annealing, to diffuse and activate the dopant in the polysilicon gate electrode without,

however, resulting in
penetration of the dopant through the barrier layer of
silicon and nitrogen
into the underlying gate oxide layer or the semiconductor
substrate.